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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/737,342	MOORE ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50 and 55-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50 and 55-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2001 and 24 June 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-50 and new claims 55-59 have been considered. Claims 4, 6, 16, 29, 31, and 41 have been amended as per Applicant's request. Claims 51-54 have been canceled as per Applicant's request. New claims 55-59 have been added as per Applicant's request.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the apparatus of claim 1, specifically the plurality of addressable registers, first comparison circuit, second comparison circuit, and dispatch circuit, and data processing system of claim 26, specifically the plurality of addressable registers, first comparison circuit, second comparison circuit, and dispatch circuit, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

3. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 55-59 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The Examiner was unable to

locate sections of the specification in which detailed description of load and store operations behaving in the manner described in the claims.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 55-59 recites the limitations regarding the operation of load and store instructions. There is insufficient antecedent basis for this limitation in the claim. Detailed disclose in the specification could not be located.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-12 and 14-25 are rejected under 35 U.S.C. 102(b) as being taught by Tran et al., U.S. Patent Number 5,764,946 (herein referred to as Tran).

10. Referring to claim 1, Tran has taught an apparatus for managing operations in a processor (Tran column 6, line 52 to column 7, line 14), said apparatus comprising:

a. A plurality of addressable registers, each of said registers partitioned into plurality of data entry fields (Tran column 1, line 49 to column 2, line 25);

b. A first comparison circuit, said first comparison circuit operable to scan and compare a value in a set of said data entry fields to a predetermined input value (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to

column 81, line3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 40 Figure 44; and Figure 46);

c. A second comparison circuit, said second comparison circuit operable to compare a first register address corresponding to a comparison match of said first comparison circuit to a second register address (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 40 Figure 44; and Figure 46); and

d. A dispatch circuit operable to dispatch data of a second data entry field of a second register corresponding to said second register address to an operation unit in response to a decode of data in a third data entry field of said second register and a comparison match of said second comparison circuit (Tran column 106, line 35 to column 107, line 62; Figure 48; and Figure 49).

11. Referring to claim 2, Tran has taught wherein said operations are Load and Store operations within said processor (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; Figure 38; Figure 39; and Figure 40).

12. Referring to claim 3, Tran has taught wherein said predetermined input value is a real address requesting particular data corresponding to one of a Load and a Store operation (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; Figure 38; Figure 39; and Figure 40).

13. Referring to claim 4, Tran has taught wherein said first scan comparison circuit comprises multiple like entry comparison circuits, each of said multiple like entry comparison

circuits operable concurrently in parallel (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; Figure 38; Figure 39; and Figure 40).

14. Referring to claim 5, Tran has taught wherein said operation unit comprises an Instruction Management Unit (IMU) (Trans column 6, line 52 to column 8, line 57 and Figure 1).

15. Referring to claim 6, Tran has taught wherein said operation unit comprises a Storage Management Unit (SMU) said SMU comprising data cache memory and controller and a Storage Reference Buffer (SRB) (Tran column 10, line 66 to column 11, line 15; column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; Figure 1; Figure 38; Figure 39; and Figure 40).

16. Referring to claim 7, Tran has taught wherein one of said data entry fields is a Valid bit field, said Valid bit field indicating whether other data entry fields are valid (Applicant's claims 7 and 32) (Tran column 123, lines 2-15 and Figure 55).

17. Referring to claim 8, Tran has taught wherein one of said data entry fields is an Instruction Identification (ID) field corresponding to a particular Load and Store operation (Tran column 123, lines 2-15 and Figure 55).

18. Referring to claim 9, Tran has taught wherein one of said data entry fields is an Instruction status field corresponding to a status of one of said Load and Store operations (Tran column 123, lines 2-15 and Figure 55).

19. Referring to claim 10, Tran has taught wherein one of said data entry fields is a Load/Store field having a Load/Store bit, said Load/Store bit corresponding to a Load operation if said Load/Store bit has a first logic state and corresponding to a Store operation if said Load/Store bit has a second logic state (Tran column 123, lines 2-15 and Figure 55).

20. Referring to claim 11, Tran has taught wherein one of said data entry fields comprises Real Address field, said Real Address field corresponding to a particular Real Address of memory data (Tran column 123, lines 2-15 and Figure 55).

21. Referring to claim 12, Tran has taught wherein one of said data entry fields is a Quadword field, said Quadword field comprising multiple bytes of data (Tran column 123, lines 2-15 and Figure 55). In regards to Tran, he has taught the data is present in an entry field. The size of the field is not a patentable distinction.

22. Referring to claim 14, Tran has taught wherein said operation unit is a pipeline execution unit operating concurrently on a plurality of said data entry fields (Tran column 10, lines 17-55 and Figure 1).

23. Referring to claim 15, Tran has taught wherein said addressable registers are addressed using a plurality of address pointers (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 40 Figure 44; and Figure 46).

24. Referring to claim 16, Tran has taught wherein said addressable registers are configured as a Storage Reference Buffer (SRB) (Tran column 10, line 66 to column 11, line 15; column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; Figure 1; Figure 38; Figure 39; and Figure 40).

25. Referring to claim 17, Tran has taught wherein one of said address pointers is a third pointer, said third pointer pointing to one of said addressable registers whose data entry fields contain data defining an earliest Store operation that is either unresolved or that matches a register address of a current Load operation (Tran column 70, lines 7-44 and Figure 36).

26. Referring to claim 18, Tran has taught wherein said address pointers comprise a fourth and a fifth pointer, said fourth and fifth pointers defining a window of register addresses from which a Load operation may be satisfied without having to access other memory storage (Tran column 70, lines 7-44 and Figure 36).

27. Referring to claim 19, Tran has taught wherein said second register address is selected from registers addresses which fall within a window of register addresses, said window of addresses defined by said address pointers (Tran column 70, lines 7-44; column 81, lines 1-3; and Figure 36).

28. Referring to claim 20, Tran has taught wherein one of said address pointers is a first pointer, said first pointer pointing to an IN register address of a first available register into which data may be added (Tran column 70, lines 7-44 and Figure 36).

29. Referring to claim 21, Tran has taught wherein one of said address pointers is a second pointer, said second pointer pointing to an OUT register address of a first available register from which register data may be retired (Tran column 70, lines 7-44 and Figure 36).

30. Referring to claim 22, Tran has taught wherein said data entry fields, added to said SRB after a mis-predicted branch instruction occurs in said processor, are retired and said first pointer is indexed to first register address of a register with added register data entry bits which were added immediately prior to said mis-predicted branch instructions (Tran column 82, line 63 to column 83, line 22).

31. Referring to claim 23, Tran has taught wherein said window of register addresses defines active Load and Store operations (Applicant's claims 23 and 48) (Tran column 70, lines 7-44 and Figure 36).

32. Referring to claim 24, Tran has taught wherein said first pointer is indexed by one when said register data has been added, said first pointed having a minimum and a maximum value wherein a decrement down from a minimum value results in said maximum value and an increment up from said maximum value results in said minimum value (Tran column 70, lines 7-44 and Figure 36).

33. Referring to claim 25, Tran has taught wherein said second pointer is indexed by one when register entry bits have been deleted, said second pointer having a minimum and a maximum value wherein a decrement down from said minimum value results in said maximum value and an increment up from said maximum value results in said minimum value (Tran column 70, lines 7-44 and Figure 36).

34. Referring to claim 55, Tran has taught wherein the SRB comprises the plurality of addressable registers (Tran column 10, line 66 to column 11, line 15; column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; Figure 1; Figure 38; Figure 39; and Figure 40).

35. Referring to claim 56, Tran has taught wherein a Load operation in one of the Load and Store operations comprises:

a. Issuing concurrently a fetch instruction requesting a real address to a data cache and the Storage Reference Buffer (SRB), the real address corresponding to an address of multiple bytes of data (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 40 Figure 44; and Figure 46);

b. Scanning the addressable registers in the SRB for the real address (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 40 Figure 44; and Figure 46);

c. Receiving the multiple bytes of data from the SRB if the real address is available (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 40 Figure 44; and Figure 46);

d. Retrieving the multiple bytes of data first from the SRB if the real address is available and second from the data cache if the real address is not available in the SRB (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 40 Figure 44; and Figure 46); and

e. Updating a corresponding one of the addressable registers with the multiple bytes of data (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 40 Figure 44; and Figure 46).

36.

Claim Rejections - 35 USC § 103

37. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

38. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tran et al., U.S. Patent Number 5,764,946 (herein referred to as Tran), as applied to claim 1 above, in view of Jerry M. Rosenberg's Dictionary of Computers, Information Processing & Telecommunications Second Edition ©1987 (herein referred to as Rosenberg). Tran has not explicitly taught wherein one of said data entry fields is an Operand Mask field, said Operand Mask field defining selected bytes of data within a selected one of said data entry fields. However, Tran has taught miscellaneous control fields (Tran column 123, lines 2-15 and Figure 55). Rosenberg has explicitly taught a mask field (Rosenberg page 370). A person of ordinary skill in the art would have recognized that a mask field describes certain data needed while ignoring unnecessary data, thereby ensuring the unnecessary data does not affect the system. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the mask field of Rosenberg in the device of Tran.

39. Claims 26-37 and 19-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tran et al., U.S. Patent Number 5,764,946 (herein referred to as Tran) in view of Kenneth L. Short's Microprocessors and Programmed Logic ©1981 (herein referred to as Short).

40. Referring to claim 26, Tran has taught a data processing system, comprising:

a. A central processing unit (CPU) (Tran column 6, lines 42-55);

b. Said CPU comprising an apparatus for managing operations in a processor (Tran column 6, line 52 to column 7, line 14), said apparatus comprising:

i. A plurality of addressable registers, each of said registers partitioned into a plurality of data entry fields (Tran column 1, line 49 to column 2, line 25);

ii. A first comparison circuit, said first comparison circuit operable to scan and compare a value in a set of said data entry fields to a predetermined input value (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 40 Figure 44; and Figure 46);

iii. A second comparison circuit, said second comparison circuit operable to compare a first register address corresponding to a comparison match of said first comparison circuit to a second register address (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 40 Figure 44; and Figure 46); and

iv. A dispatch circuit operable to dispatch data of a second data entry field of a second register corresponding to said second register address to an operation unit in response to a decode of data in a third data entry field of said second register and a comparison match of said second comparison circuit (Tran column 106, line 35 to column 107, line 62; Figure 48; and Figure 49).

41. Tran has not taught a microprocessor comprising:

a. Random access memory (RAM);

b. Read only memory (ROM);

c. An I/O adapter; and

d. A bus system coupling devise internal to said CPU.

42. However, Tran has taught a microprocessor system (Tran Abstract, line 1 and column 1, line 19-22). Short has taught a microprocessor comprising:

a. Random access memory (RAM) (Short pages 12-13 and 72-76);

b. Read only memory (ROM) (Short pages 12-13 and 72-76);

c. An I/O adapter (Applicant's claim 10); and

d. A bus system coupling devise internal to said CPU (Short pages 12-13 and 72-76).

43. A person of ordinary skill in the art at the time the invention was made would have recognized that a typical computer system incorporates these elements, thereby ensuring that output data is produced, which is a specified function of an input data (Short page 72). Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the above elements of Short in the device of Rosenberg.

44. Referring to claim 27, Tran has taught wherein said operations are Load and Store operations within said processor (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; Figure 38; Figure 39; and Figure 40).

45. Referring to claim 28, Tran has taught wherein said predetermined input value is a real address requesting particular data corresponding to one of a Load and a Store operation (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; Figure 38; Figure 39; and Figure 40).

46. Referring to claim 29, Tran has taught wherein said first scan comparison circuit comprises multiple like entry comparison circuits, each of said multiple like entry comparison

circuits operable concurrently in parallel (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; Figure 38; Figure 39; and Figure 40).

47. Referring to claim 30, Tran has taught wherein said operation unit comprises an Instruction Management Unit (IMU) (Trans column 6, line 52 to column 8, line 57 and Figure 1).

48. Referring to claim 31, Tran has taught wherein said operation unit comprises a Storage Management Unit (SMU) said SMU comprising data cache memory and controller and a Storage Reference Buffer (SRB) (Tran column 10, line 66 to column 11, line 15; column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; Figure 1; Figure 38; Figure 39; and Figure 40).

49. Referring to claim 32, Tran has taught wherein one of said data entry fields is a Valid bit field, said Valid bit field indicating whether other data entry fields are valid (Applicant's claims 7 and 32) (Tran column 123, lines 2-15 and Figure 55).

50. Referring to claim 33, Tran has taught wherein one of said data entry fields is an Instruction Identification (ID) field corresponding to a particular Load and Store operation (Tran column 123, lines 2-15 and Figure 55).

51. Referring to claim 34, Tran has taught wherein one of said data entry fields is an Instruction status field corresponding to a status of one of said Load and Store operations (Tran column 123, lines 2-15 and Figure 55).

52. Referring to claim 35, Tran has taught wherein one of said data entry fields is a Load/Store field having a Load/Store bit, said Load/Store bit corresponding to a Load operation if said Load/Store bit has a first logic state and corresponding to a Store operation if said Load/Store bit has a second logic state (Tran column 123, lines 2-15 and Figure 55).

53. Referring to claim 36, Tran has taught wherein one of said data entry fields comprises Real Address field, said Real Address field corresponding to a particular Real Address of memory data (Tran column 123, lines 2-15 and Figure 55).

54. Referring to claim 37, Tran has taught wherein one of said data entry fields is a Quadword field, said Quadword field comprising multiple bytes of data (Tran column 123, lines 2-15 and Figure 55). In regards to Tran, he has taught the data is present in an entry field. The size of the field is not a patentable distinction.

55. Referring to claim 39, Tran has taught wherein said operation unit is a pipeline execution unit operating concurrently on a plurality of said data entry fields (Tran column 10, lines 17-55 and Figure 1).

56. Referring to claim 40, Tran has taught wherein said addressable registers are addressed using a plurality of address pointers (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 40 Figure 44; and Figure 46).

57. Referring to claim 41, Tran has taught wherein said addressable registers are configured as a Storage Reference Buffer (SRB) (Tran column 10, line 66 to column 11, line 15; column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; Figure 1; Figure 38; Figure 39; and Figure 40).

58. Referring to claim 42, Tran has taught wherein one of said address pointers is a third pointer, said third pointer pointing to one of said addressable registers whose data entry fields contain data defining an earliest Store operation that is either unresolved or that matches a register address of a current Load operation (Tran column 70, lines 7-44 and Figure 36).

59. Referring to claim 43, Tran has taught wherein said address pointers comprise a fourth and a fifth pointer, said fourth and fifth pointers defining a window of register addresses from which a Load operation may be satisfied without having to access other memory storage (Tran column 70, lines 7-44 and Figure 36).

60. Referring to claim 44, Tran has taught wherein said second register address is selected from registers addresses which fall within a window of register addresses, said window of addresses defined by said address pointers (Tran column 70, lines 7-44; column 81, lines 1-3; and Figure 36).

61. Referring to claim 45, Tran has taught wherein one of said address pointers is a first pointer, said first pointer pointing to an IN register address of a first available register into which data may be added (Tran column 70, lines 7-44 and Figure 36).

62. Referring to claim 46, Tran has taught wherein one of said address pointers is a second pointer, said second pointer pointing to an OUT register address of a first available register from which register data may be retired (Tran column 70, lines 7-44 and Figure 36).

63. Referring to claim 47, Tran has taught wherein said data entry fields, added to said SRB after a mis-predicted branch instruction occurs in said processor, are retired and said first pointer is indexed to first register address of a register with added register data entry bits which were added immediately prior to said mis-predicted branch instructions (Tran column 82, line 63 to column 83, line 22).

64. Referring to claim 48, Tran has taught wherein said window of register addresses defines active Load and Store operations (Applicant's claims 23 and 48) (Tran column 70, lines 7-44 and Figure 36).

65. Referring to claim 49, Tran has taught wherein said first pointer is indexed by one when said register data has been added, said first pointed having a minimum and a maximum value wherein a decrement down from a minimum value results in said maximum value and an increment up from said maximum value results in said minimum value (Tran column 70, lines 7-44 and Figure 36).

66. Referring to claim 50, Tran has taught wherein said second pointer is indexed by one when register entry bits have been deleted, said second pointer having a minimum and a maximum value wherein a decrement down from said minimum value results in said maximum value and an increment up from said maximum value results in said minimum value (Tran column 70, lines 7-44 and Figure 36).

67. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tran et al., U.S. Patent Number 5,764,946 (herein referred to as Tran) in view of Kenneth L. Short's Microprocessors and Programmed Logic ©1981 (herein referred to as Short), as applied to claim 26 above, in view of Jerry M. Rosenberg's Dictionary of Computers, Information Processing & Telecommunications Second Edition ©1987 (herein referred to as Rosenberg). Tran has not explicitly taught wherein one of said data entry fields is an Operand Mask field, said Operand Mask field defining selected bytes of data within a selected one of said data entry fields. However, Tran has taught miscellaneous control fields (Tran column 123, lines 2-15 and Figure 55). Rosenberg has explicitly taught a mask field (Rosenberg page 370). A person of ordinary skill in the art would have recognized that a mask field describes certain data needed 5while ignoring unnecessary data, thereby ensuring the unnecessary data does not affect the system.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the mask field of Rosenberg in the device of Tran.

68. Claims 57-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tran et al., U.S. Patent Number 5,764,946 (herein referred to as Tran), as applied to claim 55 above, in view of Chang et al., U.S. Patent Number 5,835,962 (herein referred to as Chang).

69. Referring to claim 57, Tran has taught updating corresponding data entry fields in one of the addressable registers in the SRB (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; Figure 38; Figure 39; and Figure 40). Tran has not taught wherein a Store operation in one of the Load and Store operations comprises:

a. Issuing a real address generation instruction;

b. Looking up the real address in a table lookup buffer;

c. Sending the real address to a miss resolution processor if the real address is not in the table lookup buffer, the miss resolution processor determining a translated real address;

d. Sending the real address from one of the miss resolution processors and the table lookup buffer to the SRB.

70. Chang has taught

a. Issuing a real address generation instruction (Chang column 2, line 66 to column 3, line 28);

b. Looking up the real address in a table lookup buffer (Chang column 2, line 66 to column 3, line 28);

c. Sending the real address to a miss resolution processor if the real address is not in the table lookup buffer, the miss resolution processor determining a translated real address (Chang column 2, line 66 to column 3, line 28);

d. Sending the real address from one of the miss resolution processors and the table lookup buffer to the SRB (Chang column 2, line 66 to column 3, line 28).

71. A person of ordinary skill in the art at the time the invention was made, and as supported by Chang, would have recognized that it translates from virtual addresses to physical addresses in one stage (Chang column 2, lines 59-64), thereby increasing the speed and efficiency of the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the table lookup buffer of Chang in the device of Tran to increase processor speed and efficiency.

72. Referring to claims 58-59, Tran has taught

a. Sending concurrently, a request for a multiple byte word with the address to the SRB and a data cache (Applicant's claims 58 and 59) (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 40 Figure 44; and Figure 46);

b. Receiving the multiple byte word from one of the addressable registers in the Storage Reference Buffer and from a data cache (Applicant's claims 58 and 59) (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 40 Figure 44; and Figure 46);

c. Updating the multiple byte word from the data cache with an operand mask (Applicant's claims 58) (Tran column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; column 75, lines 24-42; Figure 38; Figure 39; and Figure 40);

d. Receiving from the first instruction unit store data operand (Applicant's claims 58) (Tran column 106, line 35 to column 107, line 62; Figure 48; and Figure 49);

e. Aligning the store data operand to the multiple bytes of data (Applicant's claims 58) (Tran column 106, line 35 to column 107, line 62; Figure 48; and Figure 49); and

f. Updating the multiple bytes of data with a complement of the operand mask (Applicant's claims 58) (Tran column 75, lines 24-42; column 106, line 35 to column 107, line 62; Figure 48; and Figure 49).

g. Extracting selected bytes from the multiple byte word (Applicant's claims 59) (Tran column 106, line 35 to column 107, line 62; Figure 48; and Figure 49);

h. Receiving the selected bytes by the first instruction unit (Applicant's claims 59); and

i. Updating the multiple bytes of data with a complement of the operand mask (Applicant's claims 59) (Tran column 75, lines 24-42; column 106, line 35 to column 107, line 62; Figure 48; and Figure 49).

73. Tran has not taught

a. Issuing an address generation instruction by a first instruction unit generating a real address in memory (Applicant's claims 58 and 59);

b. Updating the real address in a real address field of one of the addressable registers in the SRB (Applicant's claims 58 and 59).

74. Chang has taught

a. Issuing an address generation instruction by a first instruction unit generating a real address in memory (Applicant's claims 58 and 59) (Chang column 2, line 66 to column 3, line 28);

b. Updating the real address in a real address field of one of the addressable registers in the SRB (Applicant's claims 58 and 59) (Chang column 2, line 66 to column 3, line 28).

75. A person of ordinary skill in the art at the time the invention was made, and as supported by Chang, would have recognized that it translates from virtual addresses to physical addresses in one stage (Chang column 2, lines 59-64), thereby increasing the speed and efficiency of the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the table lookup buffer of Chang in the device of Tran to increase processor speed and efficiency.

Response to Arguments

76. Examiner withdraws objections to the specification in favor of the amended specification and replacement drawings.

77. Examiner withdraws objections to the drawings except for the objection pertaining to the drawings must show every feature of the invention specified in the claims in favor of the amended specification and replacement drawings. The drawing objection pertaining to the

drawings must show every feature of the invention specified in the claims is maintained for the reasons stated below.

78. Examiner finds the arguments regarding the 35 U.S.C. §112 first paragraph and second paragraph persuasive and withdraws these rejections.

79. Applicant's arguments filed 24 June 2004 have been fully considered but they are not persuasive.

80. Regarding the maintained drawing objection (please the section labeled "Drawings" for the complete objection), the arguments have not been found unpersuasive. The cited sections shows where the invention is disclosed in the specification but not in the drawings. The claims are directed towards an apparatus, i.e. circuit type device, but no apparatus in the drawings shows an apparatus with the claimed elements. The apparatus drawings show at best a Storage Reference Buffer (SRB) in the device, but the drawings lack the addressable registers, two comparison circuits, and dispatch circuit. There are no drawings showing how these elements are connected in an apparatus. The state diagrams shown do not detail these steps and how they are interrelated as well. The state diagrams just generically shown a broad overview of steps, but there is no state diagram showing the filter operations alluded to in the description of Figure 10. Also, state diagrams are accepted drawings for method claims not apparatus claims. §1.83(a) explicitly states, "The drawing in a nonprovisional application must show every feature of the invention specified in the claims." The current drawings do NOT show every feature of the claimed invention. The claims seem to be focused on the filters disclosed on page 14, lines 23 through page 15, line 19, but there is no drawing of these features. The mere presence of a box labeled "SRB" does not constitute the presence of the addressable registers, two comparators,

and dispatch unit. These details of the "SRB" must be shown, because they are the claimed features. Should the Applicant or Applicant's representative have questions regarding this matter, please contact the Examiner.

81. Applicant argues in essence on page 34

> "When the first comparison circuit finds a value in the data entry fields that matches the predetermined input value there is a comparison match and a corresponding first register address results. The second comparison circuit (Element 3) then compares the first register address to a second register address."

82. This has not been found persuasive. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the first register address is a result of the first comparison match and used as one of the inputs for the second comparison) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Claim 1 recites "a first register address corresponding to a comparison match of said first comparison circuit". When interpreting this claim in the broadest sense, this means that the first register address is not necessarily the result of the first comparison, but only related to the first comparison's result in some manner.

83. In general, Applicant argues on pages 35-58

> "The Applicant respectfully asserts that the Examiner has failed to point out which of these multiplicity of units making up super scalar microprocessor 200 he considers is the apparatus of Claim 1 of the present invention...For a reference to

anticipate a claimed invention, the reference must disclose every aspect of the claimed invention. The identical invention must be shown in as complete detail as is contained in the claim."

84. This has not been found persuasive. Applicant and/or Applicant's representative has not explained how these aspects of the invention are not found in the reference or how the Examiner has failed to point out which elements are considered the invention. The Examiner cited lines and column numbers relating to each element of the claims. The Examiner can only maintain the rejection and reiterate that these elements are taught in Tran. The Examiner has provided an explanation of how Tran reads upon the limitations in question in the independent claims below for further clarification of the rejections to the independent claims. Should the Applicant or Applicant's representative have any questions regarding the reference, please contact the Examiner directly to schedule an interview to clarify the prior art used.

85. The preamble of claim 1 recites "an apparatus for managing operations in a processor" and Tran, column 6, line 52 to column 7, line 14, has been cited by the Examiner. Tran has taught a superscalar microprocessor that executes operations fetched from a main memory subsystem. The superscalar microprocessor effectively manages the operations in order to execute them, since it must, in general, fetch the instructions, decode the instructions, execute the instruction, and then retire the instructions.

86. Tran, column 1, line 49 to column 2, line 25, has taught "a plurality of addressable registers, each of said registers partitioned into plurality of data entry fields". Tran has described an instruction cache with blocks of storage locations storing multiple bytes of information, i.e. multiple data entry fields. The caches are organized into rows and columns and indexed by

address bits. This means that address bits are used to find the correct block of storage containing the instruction. A cache is a small fast memory made up of high-speed data elements, like a register, which is one of a small number of high-speed memory locations. Please see InstantWeb's "cache" and "register" definitions for more information.

87. Tran, column 77, lines 33-47; column 79, lines 24-55; column 80, line 5 to column 81, line3; column 101, lines 45-60; column 102, lines 17-59; Figure 38; Figure 39; Figure 40 Figure 44; and Figure 46, has taught "a first comparison circuit, said first comparison circuit operable to scan and compare a value in a set of said data entry fields to a predetermined input value" and "a second comparison circuit, said second comparison circuit operable to compare a first register address corresponding to a comparison match of said first comparison circuit to a second register address". These lines describe how the stack cache and LOROB behave together in order to check for dependencies for load and store operations. As stated in Tran in column 77, lines 37-38, there must be a hit in the LOROB as well as a hit in the stack cache for dependency checking. In order for a hit to occur, the comparators must scan the LOROB and stack cache to see if there is a match between the input address, or predetermined input value, with an entry in the LOROB and stack cache. To simplify Tran, the first hit, resulting from a scan and comparison, occurs between the input address and the elements in the LOROB. After a hit has occurred there, it must determine whether the input address is a hit with an element in the stack cache. That means that the result of the first comparison influences whether the second comparison even takes place, i.e. the second comparison corresponds to a comparison match of the first comparator.

88. Tran, column 106, line 35 to column 107, line 62; Figure 48; and Figure 49, has taught "a dispatch circuit operable to dispatch data of a second data entry field of a second register corresponding to said second register address to an operation unit in response to a decode of data in a third data entry field of said second register and a comparison match of said second comparison circuit". Each instruction comprises tags, operands, and an opcode, i.e. data entry fields. The processor dispatches instructions to reservation stations and functional units based upon the opcodes, which must be decoded before they can correctly be dispatched. The reservation stations only dispatch instructions when all the operands are present, so some decoding must have been present in order to determine what the operands are and whether they are present or not. Tran also states in column 107, lines 25-37 that the instruction is dispatched to a functional unit from a reservation station when it has determined that all the operands, coming from the LOROB and Stack Cache, are present and there is no higher priority instruction. The comparators above checked for instruction dependencies, which, if they were both hits, means there is something of higher priority. The comparators also checked if the data was available in the LOROB and Stack Cache, thereby determining if the operands were available from them.

Conclusion

89. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

90. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

91. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596 or (571) 272-4163 after 12 October 2004. The examiner can normally be reached on M-T 7:30am-5:00pm.

92. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712 or (571) 272-9712 after 12 October 2004. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

93. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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October 1, 2004

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